REMARKS

The Examiner's Action mailed on May 6, 2003 has been received and its contents carefully considered.

In this Amendment, Applicant has cancelled claims 2, 5, 6, 9 and 10 and amended claims 1, 3, 4, 24 and 26. Claims 1, 24 and 26 are the independent claims. Claims 1, 3, 4, 7, 8, 11~13, 24 and 26 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Initially, it is noted that this Amendment has been prepared using the requested new format. If there are any irregularities in this format, it would be greatly appreciated if Applicant's Counsel would be so advised.

The Examiner has rejected claims 1~4, 7, 8, 11 and 12 as being obvious over *Yamashita et al.* (USP 5,726,493) in view of *Farnworth et al.* (USP 6,451,624). Because claim 2 has been cancelled, Applicant will treat this rejection as applying only to pending claims 1, 3, 4, 7, 8, 11 and 12. It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Applicant's independent claim 1 recites that the conductive wire has an exposed end which is substantially level with a top surface of the resin layer. The exposed end of the conductive wire is adapted to receive a first solder ball directly thereon. Further, a second solder ball is directly bonded to a first electrode. When the first solder ball is received on the exposed end of the conductive wire, the first solder ball will be disposed in alignment with the second solder ball, and the second solder ball will be electrically connected to the first solder ball, thereby allowing the first substrate to be connected to another substrate, with the first substrate having a same orientation as the another

substrate. This claimed configuration results in a structure that allows the solder balls to be stably arranged. Further, this claimed configuration allows three-dimensional mounting to be easily achieved. That is, because of the claimed configuration, when first solder ball is received on the exposed end of the conductive wire, the first solder ball will be disposed in alignment with the second solder ball. Thus, another substrate that includes such first solder balls can be easily stacked on the claimed substrate, without requiring a change in the orientation of the substrates, i.e., there is no need to turn one of the substrates upside down in order to mount the substrates together.

Further, since the exposed end of the conductive wire is substantially level with a top surface of the resin layer, when the first solder ball is received on the exposed end of the conductive wire, a more reliable connection ensues. If the exposed end of the conductive wire were recessed within the resin layer, it would be more difficult to obtain an electrical connection between the first solder ball and the conductive wire. Alternatively, if the exposed end of the conductive wire projected above the resin layer, the resin ball would essentially need to be balanced on top of the conductive wire during its connection thereto. This would result in a difficult to achieve connection process, and a connection that could easily be broken. Applicant's claimed arrangement overcomes these problems.

Yamashita et al. disclose a semiconductor device in which a printed circuit base 11 has electrode patterns (not shown) disposed on opposite sides thereof. Solder balls are connected to the electrode patterns disposed on the lower surface. Further, through holes 15 are connected to the electrode patterns of the lower surface (column 5, lines 36-37), and are connected to the electrode patterns of the upper surface (column 5,

lines 30-32). This reference also teaches providing electrode members 17, which have top ends which either protrude from, or are recessed within a sealing resin 16. The lower ends of the respective electrode members are inserted into the through holes 15 (column 5, lines 50-52). This reference discloses that this configuration allows for the electrode members 17 to be electrically connected to outer terminals outside of the sealing resin 16 (see column 6, lines 1-4).

However, and in contrast to the present invention, this reference fails to disclose or suggest that when a first solder ball is received on the exposed end of the conductive wire, the first solder ball will be disposed in alignment with the second solder ball. Instead, this reference teaches that the electrode members 17 are disposed in alignment with the respective holes 15, but that the solder balls 13 are connected to the holes 15 using the electrode patterns. This implies that the solder balls 13 are disposed to be offset relative to the holes 15, and thus also offset relative to the electrode members 17. It is also noted that the embodiment shown in Figure 11 does not teach this claimed alignment. Instead, this reference teaches that the embodiment shown in Figure 11 is based on the first embodiment. Thus, one can logically assume that the upper solder balls are offset, front to back, relative to the lower solder balls, so that the solder balls are not disposed in alignment as required by claim 1.

Moreover, claim 1 requires that the first substrate have a same orientation as the another substrate, and that the exposed end of the conductive wire and the top surface of the resin layer are substantially level with each other, with the exposed end of the conductive wire being adapted to receive a first solder ball directly thereon. The only embodiment of the cited reference that teaches arranging the devices with the same

orientation is shown in Figure 11. However, this embodiment requires that the electrodes project beyond the surface of the resin 16, so that the resulting stacked configuration does not have the stability or reliability of Applicant's claimed device. For example, the upper semiconductor device could be easily dislocated from the lower semiconductor device.

The Examiner's Action also acknowledges that the cited reference does not teach forming electrode members such that they are level with the top of the sealing resin, and relies on the teachings of *Farnworth et al.* to overcome this admitted deficiency. However, it is initially noted that *Yamashita et al.* specifically teach away from modifying the electrode members 17 so that the electrode members 17 would have an exposed end that is substantially level with a top of the sealing resin 16. The Examiner's attention is particularly directed to column 6, lines 1-4 and column 7, lines 19-21 of this reference, where this reference discloses that this configuration allows for the electrode members 17 to be electrically connected to outer terminals outside of the sealing resin 16. The Examiner's attention is also directed to the discussion of the embodiments shown in Figures 7, 8 and 10, where this reference teaches that the heat release member 41, 51 is provided with penetration holes for receiving the portion of the electrode members 17 that extends above the sealing resin (see column 8, line 58 through column 9, line 7; column 9, lines 48-54; and column 10, lines 7-12). As is apparent from these noted passages, this reference specifically provides that, for these embodiments, the exposed ends of the electrode members 17 are not level with the upper surface of the resin layer.

This reference also teaches that the electrodes must either project above the upper surface of the resin 16 (in the manner of electrodes 17), or be recessed below the upper surface of the resin 16 (in the manner of the electrodes 22), for various reasons, including allowing the protruding portions of the electrodes 17 to be received within the holes 23 disposed over the electrodes 22, to facilitate a stacking of the semiconductor devices (see column 11, lines 6-29, and Figures 13 and 14). Thus, since this reference specifically teaches away from modifying the electrode members 17, 22 so that the electrode members 17, 22 would have an exposed end which is substantially level with a top of the sealing resin 16, it is submitted that there would have been no motivation for one skilled in the art to have modified the electrode members 17 in a manner that would render Applicant's claim 1 obvious, irrespective of what is taught by the other cited references, except in a hindsight attempt at reconstructing Applicant's claimed invention.

Moreover, *Farnworth et al.* fail to overcome the other noted deficiencies of *Yamashita et al.* As such, it is submitted that Applicant's independent claim 1, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited references. It is thus requested that these claims be allowed and that this rejection be withdrawn.

The Examiner has further rejected claims 5, 6, 9, 10 and 13 as being obvious over *Yamashita et al.* and further in view of *Aiba et al.* (USP 6,348,728). Because claims 5, 6, 9 and 10 have been cancelled, Applicant will treat this rejection as pertaining only to claim 13. Because claim 13 depends from independent claim 1, and because *Aiba et al.* do not overcome the above-noted deficiencies of *Yamashita et al.*,

and further in view of the fact that *Yamashita et al.* teach away from modifying the electrode members 17, 22 in a manner similar to the structure required by Applicant's independent claim 1, it is submitted that this claim is patentably distinguishable over the cited references for at least the same reasons as independent claim 1, from which this claim depends, as well as for the additional features recited therein. It is thus requested that this rejection be withdrawn and that this claim be allowed.

The Examiner has rejected claim 24 as being obvious over *Yamashita et al.* and further in view of *King et al. (USP 6,429,528).* It is submitted that this claim is patentably distinguishable over the cited combination of references for at least the following reasons.

Applicant's independent claim 24 recites a semiconductor package which has a conductive wire, in which an exposed other end of the conductive wire and a top surface of the resin layer are substantially level with each other. Neither of the cited references teach this feature. Moreover, and as argued above in detail, *Yamashita et al.* teach away from modifying the electrode members 17, 22 in a manner similar to the structure required by Applicant's independent claim 24. As such, it is submitted that Applicant's independent claim 24 is patentably distinguishable over the cited references, and it is requested that this rejection be withdrawn, and that this claim be allowed.

The Examiner has rejected claim 26 as being obvious over *Yamashita et al.* and further in view of *Aiba et al.* and *Lau.* It is submitted that this claim is patentably distinguishable over the cited combination of references for at least the following reasons.

Applicant's independent claim 26 recites a semiconductor package which has a conductive wire, in which an exposed other end of the conductive wire and a top surface of the resin layer are substantially level with each other. Neither of the cited references teach this feature. Moreover, and as argued above in detail, *Yamashita et al.* teach away from modifying the electrode members 17, 22 in a manner similar to the structure required by Applicant's independent claim 26. As such, it is submitted that Applicant's independent claim 26 is patentably distinguishable over the cited references, and it is requested that this rejection be withdrawn, and that this claim be allowed.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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